

MC74LVX374

Octal D-Type Flip-Flop with 3-State Outputs

With 5V-Tolerant Inputs

The MC74LVX374 is an advanced high speed CMOS octal D-type flip-flop with 3-state outputs. The inputs tolerate voltages up to 7.0 V, allowing the interface of 5.0 V systems to 3.0 V systems.

This 8-bit D-type flip-flop is controlled by a clock input and an output enable input. When the output enable input is high, the eight outputs are in a high impedance state.

Features

- High Speed: $f_{max} = 160$ MHz (Typ) at $V_{CC} = 3.3$ V
- Low Power Dissipation: $I_{CC} = 4$ μ A (Max) at $T_A = 25^\circ$ C
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Low Noise: $V_{OLP} = 0.8$ V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300 mA
- ESD Performance:
 - Human Body Model > 2000 V;
 - Machine Model > 200 V
- Pb-Free Packages are Available*

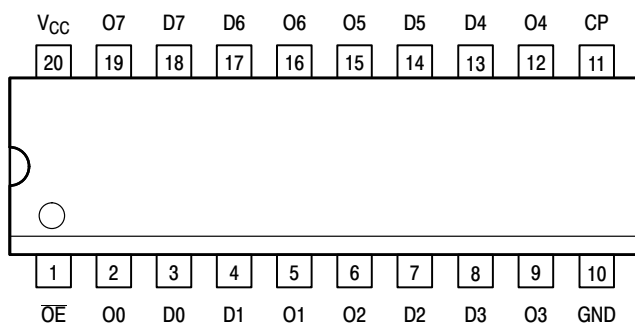


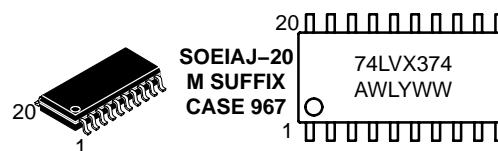
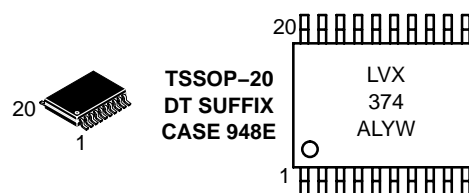
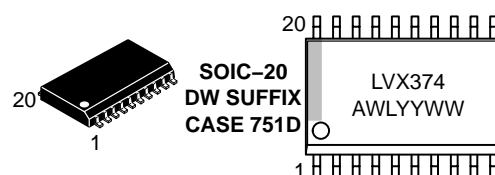
Figure 1. 20-Lead Pinout (Top View)



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MARKING DIAGRAMS



A = Assembly Location
L, WL = Wafer Lot
Y, YY = Year
W, WW = Work Week

PIN NAMES

Pins	Function
\overline{OE}	Output Enable Input
CP	Clock Pulse Input
D0-D7	Data Inputs
O0-O7	3-State Outputs

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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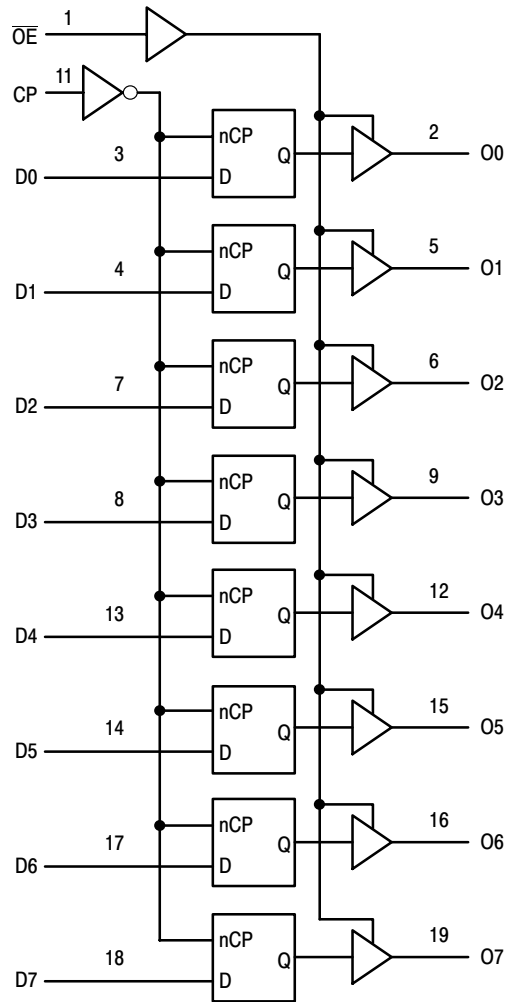


Figure 2. Logic Diagram

INPUTS			OUTPUTS	OPERATING MODE
OE	CP	Dn	On	
L L	↑ ↑	l h	L H	Load and Read Register
L	↕	X	NC	Hold and Read Register
H	↕	X	Z	Hold and Disable Outputs
H H	↑ ↑	l h	Z Z	Load Internal Register and Disable Outputs

H = High Voltage Level; h = High Voltage Level One Setup Time Prior to the Low-to-High Clock Transition; L = Low Voltage Level; l = Low Voltage Level One Setup Time Prior to the Low-to-High Clock Transition; NC = No Change, State Prior to Low-to-High Clock Transition; X = High or Low Voltage Level and Transitions are Acceptable; Z = High Impedance State; ↑ = Low-to-High Transition; ↕ = Not a Low-to-High Transition; For I_{CC} Reasons DO NOT FLOAT Inputs

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MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	-0.5 to +7.0	V
V_{in}	DC Input Voltage	-0.5 to +7.0	V
V_{out}	DC Output Voltage	-0.5 to $V_{CC} + 0.5$	V
I_{IK}	Input Diode Current	-20	mA
I_{OK}	Output Diode Current	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation	180	mW
T_{stg}	Storage Temperature	-65 to +150	$^{\circ}C$

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage	2.0	3.6	V
V_{in}	DC Input Voltage	0	5.5	V
V_{out}	DC Output Voltage	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	-40	+85	$^{\circ}C$
$\Delta t/\Delta V$	Input Rise and Fall Time	0	100	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	$T_A = 25^{\circ}C$			$T_A = -40$ to $85^{\circ}C$		Unit
				Min	Typ	Max	Min	Max	
V_{IH}	High-Level Input Voltage		2.0	1.5			1.5		V
			3.0	2.0			2.0		
			3.6	2.4			2.4		
V_{IL}	Low-Level Input Voltage		2.0			0.5		0.5	V
			3.0			0.8		0.8	
			3.6			0.8		0.8	
V_{OH}	High-Level Output Voltage ($V_{in} = V_{IH}$ or V_{IL})	$I_{OH} = -50\mu A$ $I_{OH} = -50\mu A$ $I_{OH} = -4mA$	2.0	1.9	2.0		1.9		V
			3.0	2.9	3.0		2.9		
			3.0	2.58			2.48		
V_{OL}	Low-Level Output Voltage ($V_{in} = V_{IH}$ or V_{IL})	$I_{OL} = 50\mu A$ $I_{OL} = 50\mu A$ $I_{OL} = 4mA$	2.0		0.0	0.1		0.1	V
			3.0		0.0	0.1		0.1	
			3.0			0.36		0.44	
I_{in}	Input Leakage Current	$V_{in} = 5.5V$ or GND	3.6			± 0.1		± 1.0	μA
I_{OZ}	Maximum 3-State Leakage Current	$V_{in} = V_{IL}$ or V_{IH} $V_{out} = V_{CC}$ or GND	3.6			± 0.2 5		± 2.5	μA
I_{CC}	Quiescent Supply Current	$V_{in} = V_{CC}$ or GND	3.6			4.0		40.0	μA

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AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0\text{ns}$)

Symbol	Parameter	Test Conditions	$T_A = 25^\circ\text{C}$			$T_A = -40 \text{ to } 85^\circ\text{C}$		Unit
			Min	Typ	Max	Min	Max	
f_{max}	Maximum Clock Frequency (50% Duty Cycle)	$V_{\text{CC}} = 2.7\text{V}$ $C_L = 15\text{pF}$ $C_L = 50\text{pF}$	60 45	115 60		50 40		MHz
		$V_{\text{CC}} = 3.3 \pm 0.3\text{V}$ $C_L = 15\text{pF}$ $C_L = 50\text{pF}$	100 60	160 95		85 55		
t_{PLH} , t_{PHL}	Propagation Delay CP to O	$V_{\text{CC}} = 2.7\text{V}$ $C_L = 15\text{pF}$ $C_L = 50\text{pF}$		8.5 11.0	16.3 19.8	1.0 1.0	19.5 23.0	ns
		$V_{\text{CC}} = 3.3 \pm 0.3\text{V}$ $C_L = 15\text{pF}$ $C_L = 50\text{pF}$		6.7 9.2	10.6 14.1	1.0 1.0	12.5 16.0	
t_{PZL} , t_{PZH}	Output Enable Time OE to O	$V_{\text{CC}} = 2.7\text{V}$ $R_L = 1\text{k}\Omega$ $C_L = 15\text{pF}$ $C_L = 50\text{pF}$		7.6 10.1	14.5 18.0	1.0 1.0	17.5 21.0	ns
		$V_{\text{CC}} = 3.3 \pm 0.3\text{V}$ $R_L = 1\text{k}\Omega$ $C_L = 15\text{pF}$ $C_L = 50\text{pF}$		5.9 8.4	9.3 12.8	1.0 1.0	11.0 14.5	
t_{PLZ} , t_{PHZ}	Output Disable Time $\overline{\text{OE}}$ to O	$V_{\text{CC}} = 2.7\text{V}$ $R_L = 1\text{k}\Omega$ $C_L = 50\text{pF}$		11.5	18.5	1.0	22.0	ns
		$V_{\text{CC}} = 3.3 \pm 0.3\text{V}$ $R_L = 1\text{k}\Omega$ $C_L = 50\text{pF}$		9.6	13.2	1.0	15.0	
t_{OSHL} , t_{OSLH}	Output-to-Output Skew (Note 1)	$V_{\text{CC}} = 2.7\text{V}$ $C_L = 50\text{pF}$ $V_{\text{CC}} = 3.3 \pm 0.3\text{V}$ $C_L = 50\text{pF}$			1.5 1.5		1.5 1.5	ns

1. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}); parameter guaranteed by design.

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	$T_A = 25^\circ\text{C}$			$T_A = -40 \text{ to } 85^\circ\text{C}$		Unit
		Min	Typ	Max	Min	Max	
C_{in}	Input Capacitance		4	10		10	pF
C_{out}	Maximum Three-State Output Capacitance		6				pF
C_{PD}	Power Dissipation Capacitance (Note 2)		32				pF

2. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{\text{CC(OPR)}} = C_{\text{PD}} \cdot V_{\text{CC}} \cdot f_{\text{in}} + I_{\text{CC}}/8$ (per flip-flop). C_{PD} is used to determine the no-load dynamic power consumption; $P_{\text{D}} = C_{\text{PD}} \cdot V_{\text{CC}}^2 \cdot f_{\text{in}} + I_{\text{CC}} \cdot V_{\text{CC}}$.

NOISE CHARACTERISTICS (Input $t_r = t_f = 3.0\text{ns}$, $C_L = 50\text{pF}$, $V_{\text{CC}} = 3.3\text{V}$, Measured in SOIC Package)

Symbol	Characteristic	$T_A = 25^\circ\text{C}$		Unit
		Typ	Max	
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	0.5	0.8	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	-0.5	-0.8	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		2.0	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		0.8	V

TIMING REQUIREMENTS (Input $t_r = t_f = 3.0\text{ns}$)

Symbol	Parameter	Test Conditions	$T_A = 25^\circ\text{C}$		$T_A = -40 \text{ to } 85^\circ\text{C}$		Unit
			Typ	Limit	Limit		
t_{w}	Minimum Pulse Width, CP	$V_{\text{CC}} = 2.7\text{V}$ $V_{\text{CC}} = 3.3 \pm 0.3\text{V}$		7.5 5.0	8.0 5.5		ns
t_{su}	Minimum Setup Time, D to CP	$V_{\text{CC}} = 2.7\text{V}$ $V_{\text{CC}} = 3.3 \pm 0.3\text{V}$		6.5 4.5	6.5 4.5		ns
t_{h}	Minimum Hold Time, D to CP	$V_{\text{CC}} = 2.7\text{V}$ $V_{\text{CC}} = 3.3 \pm 0.3\text{V}$		2.0 2.0	2.0 2.0		ns

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ORDERING INFORMATION

Device	Package	Shipping†
MC74LVX374DWR2	SOIC-20	1000 Tape & Reel
MC74LVX374DWR2G	SOIC-20 (Pb-Free)	1000 Tape & Reel
MC74LVX374DTR2	TSSOP-20*	2500 Tape & Reel
MC74LVX374M	SOEIAJ-20	50 Units / Rail
MC74LVX374MG	SOEIAJ-20 (Pb-Free)	50 Units / Rail
MC74LVX374MEL	SOEIAJ-20	2000 Tape & Reel
MC74LVX374MELG	SOEIAJ-20 (Pb-Free)	2000 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*This package is inherently Pb-Free.

SWITCHING WAVEFORMS

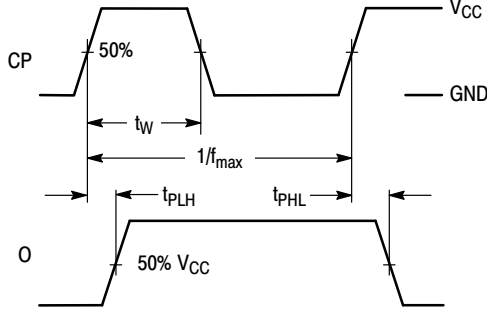


Figure 3.

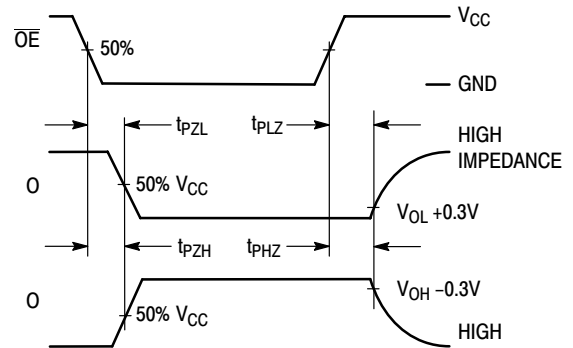


Figure 4.

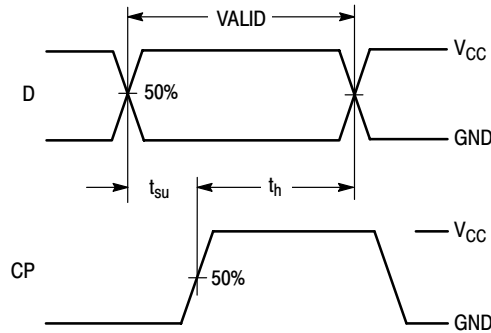
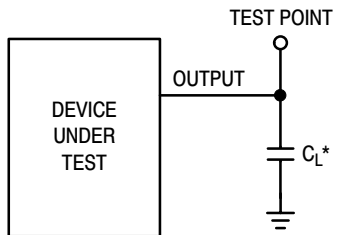


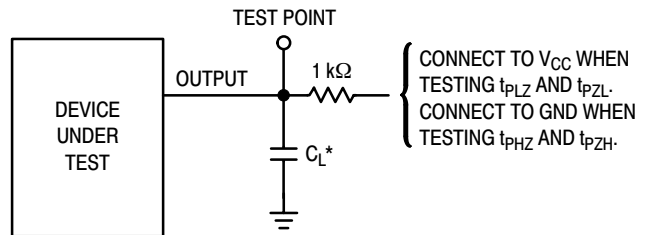
Figure 5.

TEST CIRCUITS



*Includes all probe and jig capacitance

Figure 6. Propagation Delay Test Circuit



*Includes all probe and jig capacitance

Figure 7. Three-State Test Circuit

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PACKAGE DIMENSIONS

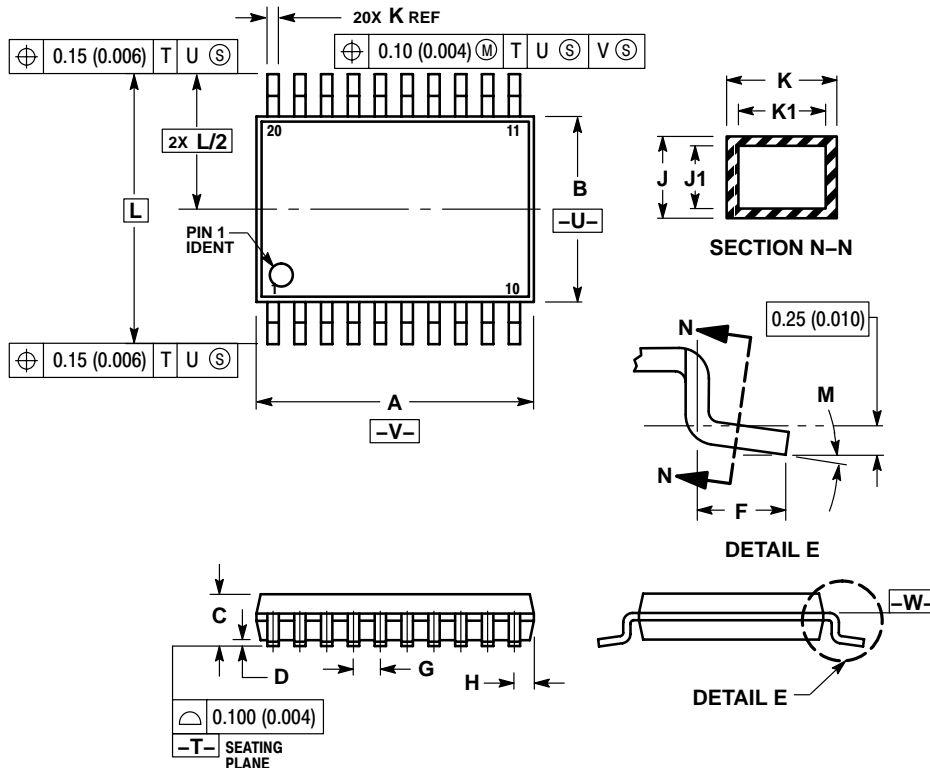
SOIC-20
DW SUFFIX
CASE 751D-05
ISSUE G



NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

TSSOP-20
DT SUFFIX
CASE 948E-02
ISSUE B



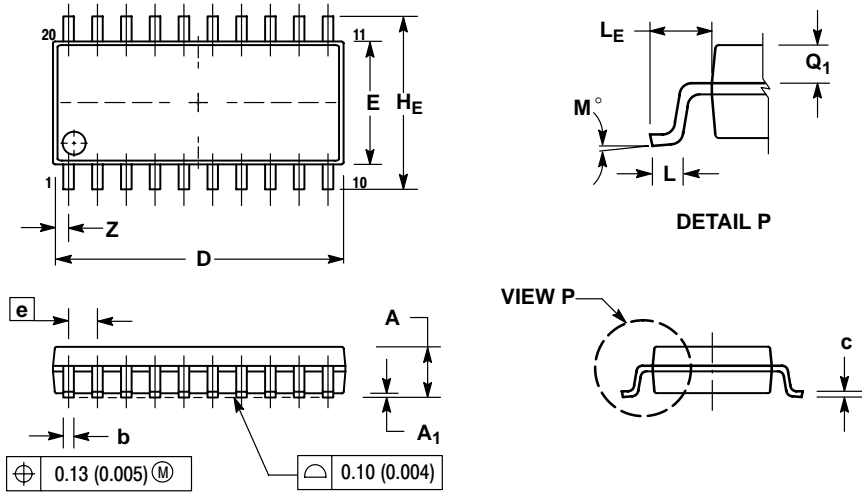
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

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PACKAGE DIMENSIONS

SOEIAJ-20
M SUFFIX
CASE 967-01
ISSUE O



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A ₁	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	12.35	12.80	0.486	0.504
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
HE	7.40	8.20	0.291	0.323
LE	0.50	0.85	0.020	0.033
L _F	1.10	1.50	0.043	0.059
M	0°	10°	0°	10°
Q ₁	0.70	0.90	0.028	0.035
Z	---	0.81	---	0.032

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